AF/2814 $

CS99-120
Serial number 09/418,029

APPEAL BRIEF

TO: COMMISIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

From : George O. Saile (Reg. No. 19,572)
28 Davis Avenue
Poughkeepsie, NY 12603

Date: February 19, 2003

REF: APPLICANT : Lap Chan
SERIAL NO. : 09/418,029
ART UNIT : 2814
FILING DATE : 10/14/99
ATT'Y NO. : CS99-120
EXAMINER : Rao, Shrinivas H.
TITLE : A NEW METHOD TO FORM A CROSS NETWORK OF AIR GAPS WITHIN IMD LAYER

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 07/16/02 and made FINAL, and to an Advisory Action, dated 11/15/02, applicants filed a notice of appeal on 12/06/2002. In accord with applicants' notice of appeal, please accept this appeal brief. No oral hearing is requested.

The Commissioner of Patents and Trademarks is hereby authorized to charge the fee of $320.00 associated with this appeal brief to Deposit Account No, 19-0033, along with any additional extension fee

02/27/2003 AWONDAF1 00000132 190033 09418029
01 FC:1402 320.00 CH

Stephen B. Ackerman, Reg. No 37,761

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D C 20231, on February 19, 2003.

Stephen B Ackerman
Name

Signature

2/19/03
Date

APPEAL BRIEF

1. Real Party in Interest

The real party in interest for this application are the assignees:

Chartered Semiconductor Manufacturing Ltd.
60 Woodlands Industrial Park D Street 2
Singapore, Singapore 738406

National University of Singapore
10, Kent Ridge Crescent
Singapore, Singapore 119260

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims:

Claims 1-3, 6-10, 12-14, 18-22 as originally filed and amended claims 4-5, 11, 16, 17 and 23-24 remain in this application. Claims 1-14 and claims 16-24 have been finally rejected under 35 U.S.C. 103(a). No claims have been allowed.

4. Status of the Amendments:

An Amendment, dated 04/23/02, which included an amendment to claims 4-5, 11, 16, 17 and 23-24, was submitted in response to a first office action and accepted. The response to the FINAL office action, dated October 15, 2002 did not include any amendments to the claims.

5. Summary of Invention:

A new method is provided for creating air gaps in a layer of IMD. A first layer of dielectric is deposited over a surface, the surface contains metal points of contact. Trenches are etched in this first layer of dielectric. The trenches are filled with a first layer of nitride or disposable solid and polished. A second layer of dielectric is deposited over the first layer of dielectric. Trenches are formed in the second layer of dielectric, the trenches created in the first and the second layers of dielectric intersect under an angle. A second layer of nitride or disposable solid is deposited over the second layer of dielectric. The layer of nitride or disposable solid is polished. A thin layer of oxide is deposited over the surface of the second layer of dielectric. The thin layer of oxide is masked and etched thereby creating openings in this thin layer of oxide, these openings align with the points of intersect of the trenches in the first layer of dielectric and in the second layer of dielectric. The nitride or removable solid is removed from the trenches. The openings in the thin layer of oxide are closed, leaving a network of trenches that is filled with air in the two layers of dielectric that now function as the Inter Level Dielectric.

The invention more specifically provides for:

- forming metal traces over a substrate
- depositing a first layer of dielectric over the substrate, thereby including the metal traces
- creating trenches in the first level of dielectric, the trenches running in a X-direction
- filling the trenches in the first layer of dielectric with a first layer of nitride or another disposable solid
- depositing a second layer of dielectric over the first layer of dielectric, thereby including the first layer of nitride or another disposable solid
- creating trenches in the second level of dielectric the trenches running in a Y-direction, the trenches furthermore having intersects with the trenches created in the first layer of dielectric
- filling the trenches in the second layer of dielectric with a second layer of nitride or another disposable solid
- depositing a first thin layer of oxide over the second layer of dielectric, thereby including the second layer of nitride or other disposable solid
- etching openings in the first thin layer of oxide, the openings to align with the intersects between the trenches

created in the first level of dielectric and the trenches created in the second layer of dielectric

- removing the second layer of nitride or other disposable solid and removing the first layer of nitride or other disposable solid from the trenches, and
- depositing a second thin layer of oxide over the first thin layer of oxide thereby closing the openings in the first thin layer of oxide.

CLAIM 1 IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

1. A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate 10 whereby the surface of said semiconductor substrate has been provided with points 12 of electrical contact;

forming a first network of nitride (16, Fig. 3a) filled trenches (15, Fig. 2b) in a first level of dielectric 14 said first level of dielectric having been deposited on the surface of said substrate 10;

forming a second network of nitride (20, Fig. 5a) filled trenches (19, Fig. 4a) in a second level of dielectric 18 said second level of dielectric (18) having been deposited on the

surface of said first level of dielectric (14) whereby furthermore said second network of nitride filled trenches is in physical contact with and intersects with said first network of nitride filled trenches, Fig. 5a;

depositing a first thin layer 22, Fig. 6a, of oxide over the surface of said second layer 18 of dielectric;

etching openings 24, Fig. 6a, in said first thin layer 22 of oxide said openings to align with said intersects between said first network of nitride filled trenches and said second network of nitride filled trenches, Fig. 6a;

removing said nitride from said second network of trenches furthermore removing said nitride from said first network of trenches, fig. 7a/7b; and

depositing a second thin layer 26, Fig. 7a/7b, of oxide over the surface of said first thin layer 22, Fig. 7a/7b, of oxide thereby closing said openings 14, fig. 7a, in said first thin layer 22, Fig. 7a/7b, of oxide.

(THIS COMPLETES FIGS. 1A-8B; SEE DESCRIPTION ON PAGES 10-19)

CLAIM 11 IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

11. A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate 10, fig. 1a, whereby the surface of said semiconductor substrate has been provided with points 12, Fig. 1a, of electrical contact;

forming a first network of trenches 15, Fig. 2a, in a first level 14, Fig. 2a, of dielectric said first level of dielectric (14) having been deposited on the surface of said substrate 10 whereby said first network of trenches 15, Fig. 2a, is filled with a disposable solid layer 16, Fig. 3a, creating a first network of disposable solid filled trenches;

forming a second network of trenches 19, Fig. 4a, in a second level of dielectric 18, Fig. 4a, said second level of dielectric 18, Fig. 4a, having been deposited on the surface of said first level of dielectric 14, Fig. 4a, whereby said second network of trenches 19 is in physical contact with and intersects with said first network 16 of a disposable solid filled trenches (Fig. 4a, 5a) whereby furthermore said second network of trenches 19 is filled with a disposable solid layer 20, Fig. 5a, creating a second network 20, Fig. 5a, of disposable solid filled trenches;

depositing a first thin layer 22, Fig. 6a, of oxide over the surface of said second layer 18, Fig. 6a, of dielectric;

etching openings 24, Fig. 6a, in said first thin layer 22, Fig. 6a, of oxide said openings 24 to align with said intersects

between said first network of trenches 16 and said second network of trenches 20, Fig. 6a;

removing said disposable solid layer from said second network of trenches 20 furthermore removing said disposable solid layer from said first network of trenches 16; and

depositing a second thin layer 26, Fig. 7a, of oxide over the surface of said first thin layer 22, Fig. 7a, of oxide thereby closing said openings 24 in said first thin layer 22 of oxide.

(THIS COMPLETES FIGS. 1A-8B; SEE DESCRIPTION ON PAGES 10-19)

CLAIM 23 IS READ ON THE SPECIFICATION AND DRAWINGS AS FOLLOWS:

23. A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate 10, Fig. 1a;

depositing a layer of metal 12, Fig. 1a, on the surface of said substrate;

etching said metal layer in a pattern to form metal leads 12, Fig. 1a, said metal leads running in a Y-direction said metal leads furthermore having top surfaces;

depositing a first layer 14 of dielectric over the surface of said substrate thereby including said metal leads 12, Fig. 1a;

creating trenches 15, Fig. 2a, in said first level of dielectric 14, Fig. 2a, said trenches running in a X-direction;

filling said trenches in said first layer of dielectric with a first layer of nitride 16, Fig. 3a, or another disposable solid;

depositing a second layer 18, Fig. 4a, of dielectric over the surface of said first layer 14, Fig. 4a, of dielectric thereby including said first layer 16, Fig. 4a, of nitride or another disposable solid;

creating trenches 19, Fig. 4a, in said second level of dielectric said trenches running in a Y-direction said trenches furthermore having intersects with said trenches 16 created in said first layer of dielectric;

filling said trenches in said second layer of dielectric with a second layer 20, Fig. 5a, of nitride or another disposable solid;

depositing a first thin layer 22, Fig. 6a, of oxide over the surface of said second layer 18, Fig. 6a, of dielectric thereby including the surface of said second layer 20, Fig. 6a, of nitride or other disposable solid;

etching openings 24, Fig. 6a, in said first thin layer 22, Fig. 6a, of oxide said openings to align with said intersects between said trenches created 15, Fig. 2a, in said first level

14 of dielectric and said trenches 19, Fig. 4a, created in said second layer 18 of dielectric;

removing said second layer 20 of nitride or other disposable solid from said trenches 19 created in said second layer 18 of dielectric furthermore removing said first layer 16 of nitride or other disposable solid from said trenches 15 created in said first layer 14 of dielectric thereby creating a network of trenches in said first layer 14 of dielectric and in said second layer 18 of dielectric whereby said trenches in said first layer 14 of dielectric intersect said trenches in said second layer 18 of dielectric under an angle of about 90 degrees, said angle of about 90 degrees being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said trenches created in said first level of dielectric and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said trenches created in said second layer of dielectric and the surface of said semiconductor substrate, said second plane having been extended towards said

surface of said semiconductor substrate to enable intersection therewith; and

depositing a second thin layer 26, Fig. 7a, of oxide over the surface of said first thin layer 22, Fig. 7a, of oxide thereby closing off said openings 24 in said first thin layer 22 of oxide.

(THIS COMPLETES FIGS. 1A-8B; SEE DESCRIPTION ON PAGES 10-19)

Dependent claims 12-14, 16-22 and 24 describe added important and critical/unexpected details based on experimental results relating to the independent claims.

6. Issues: Whether claims 1-14 and claims 16-24 are unpatentable over Katoh (US Patent 5,141,896) and Ito (US Patent 6,297,145 B1). Further, whether claims 9-10, 12-14, 21-24 are unpatentable over Katoh (US Patent 5,141,896) and Ito (US Patent 6,297,145 B1) in view of Havemann et al. (US Patent 5,461,003).

7. Grouping of Claims: Claim 1 and dependent claims 2-10 form a first group of claims, claim 11 and dependent claims 12-14 and 16-22 form a second group of claims, claim 23 and dependent claim 24 form a third group of claims.

8. ARGUMENTS

ARGUMENTS IN SUPPORT OF claims 1-14 and claims 16-24 being patentable over Katoh (US Patent 5,141,896) and Ito (US Patent 6,297,145 B1).

Regarding the first quote provided by Examiner of page 4 of the Office Action, Examiner refers to "Katoh in Fig. 2(d) etc. col. 5, lines 29-40 states:". In referring to col. 5, lines 29-40 of the specification provided by Katoh, Applicant finds that this text, col. 5, lines 29-40, describes (see col. 5, line 28) Fig. 5(g). This discrepancy does not provide a meaningful basis for Applicant to make a comparative statement since it is not clear to Applicant which figure is being described and referred to by Examiner.

Examiner states, as a last line entry on page 4 of the Office Action:

"Further, Ito in Figs. 7(a) and (b) and col. 9 lines 13-17 shows and describes structure identical to Fig. 8(a) of the instant invention."

"Identical" has the meaning of "indistinguishable", Applicant respectfully submits that this is not the case for Figs. 7(a) and (b) of Ito and Fig. 8(a) of the instant invention. Fig. 8(a) of the instant invention shows a three dimensional view of the structure created by the instant invention, with metal contacts 12, there-over created three layers of dielectric in which perpendicularly intersecting trenches, filled with air, have been created, over the surface of which a metal pattern 28 is provided.

Ito Figs. 7(a) and (b) show (two-dimensional) cross sections, specifically highlighting:

- 1, the cross section of a substrate
- 2, a first layer of metal
- 16, a first via hole, this via holes is, in accordance with the cross-hatching provided therein, filled with metal contacting 2, the first layer of metal
- 3, a first interlayer insulating film
- 20, a second level of metal interconnect, connected with the metal provided in via hole 3
- 18, a (third) silicon oxide film
- 21, a second interlayer insulating film
- 22, a (third) silicon nitride film
- 12, a second silicon oxide film

- 15, a silicon nitride film, which together with 12 form an insulation post 35.

As a sequel to the referred to Figs. 7(a) and (b), it is of interest to further follow the Ito invention to for instance Fig. 10(a), where are shown overlying layers of metal such as layers 2, 16, 20, 32 and 33. These layers are created contacting each other with a layer of metal provided in each of the levels of the cross section shown in Fig. 10(a). Contrasting this with the three dimensional view of the instant invention, shown in Fig. 8a, no metal is provide between the metal contacts 12 and the metal pattern 18, this in accordance with, as stated in the specification of the instant invention: "leaving a network of trenches that are filled with air in the two layers of dielectric that now function as the Inter Level Dielectric."

The above comparison between Ito, Figs. 7(a) and (b) and Fig. 8(a) of the instant invention hopefully has removed any notion that these two representations are identical or show structures that have any significant similarity.

It might be suggested that Katoh combined with Ito could form the basis for the instant invention. By reviewing the

essential points of these two inventions, it is suggested that such a conclusion is not obvious, as follows.

Ito provides for interconnected and overlying layers of interconnect metal, creating the overlying layers by simultaneously providing what is referred to as an air bridge construction. Katoh provides for overlying layers of interconnect metal, such as layers 2 and 6, Fig. 1 of Katoh, the overlying and adjacent layers spatially intersect separated by a "crossing point" 3 of inorganic insulating film.

By contrast, the instant invention provides for the creation of a compound layer of dielectric, layers 14, 18 and 30 of Fig. 8(a), creating trenches in the overlying layers of dielectric filled with air so that first level metal 12 can be separated from second layer metal 28 by a low-k dielectric constant layer of IMD.

Based on the above comparison, it is kindly suggested that, although all three of the inventions address the creation of interconnect metal, each of these three inventions is significantly different from the other two inventions.

Regarding claim 11 and the last paragraph that is cited by Examiner on page 5 of the Office Action, Ito uses, as is clear from the quoted description of Fig. 8(a) and 8(b), a very specific sequence of material depositions and etching, in essence to form overlying insulation posts such as posts 35 and 36 of Fig. 8(b) and overlying and interconnecting layers of metal (layers 2 and 20, Fig. 5b).

Ito will next be analyzed in some more detail, whereby it will be recognized that Ito creates a number of overlying insulating posts, such as posts 35 and 36, Fig. 10, meaning that processing cycles are repeated for the overlying posts. In the interest of brevity, only one such cycle will be highlighted, as detailed by Ito in col. 6, lines 30 e.a.

- insulating post 35, which is provided for the purpose of supporting an upper metal interconnect 20
- the insulating post is formed by a first insulating film 12 that forms the outer part of the post and a second insulating film 15 that is surrounded by the first insulating film 12
- a via hole 10 that is provided between the upper and the lower metal interconnects 2 and 20, the via hole being filled with a metal 40 for the purpose of connecting these metal interconnects.

In sum: Ito creates overlying layers of interconnect metal and, to support higher levels of metal Ito creates, off-set from the interconnect vias, supporting posts so that a stable layer of interconnect is created.

After Ito has created the insulating posts and the metal via interconnect, surrounding layer 3 of first insulation film material is removed, in fact creating an air filled environment around the insulating post (35, Fig. 5a) and the metal via (40, Fig. 5b).

Where, in response to a previous Office Action, Examiner asserts that "Applicant contends that prior art does not teach the removal of other materials from the trenches", Applicant has searched the previous response to an Office Action for this statement but has not been unable to locate any such statement.

What Applicant has stated with respect to claim 11 in response to a previous Office Action remains, even on closer review, valid, as follows:

"Claim 11 is specified in order to provide that the process of the invention can be applied using another material, other than nitride, that can also be removed from the trenches that have been created in the overlaying layers of dielectric. Claim 11 is therefore required to completely specify the method of the invention."

From the above provided detail, Applicant respectfully submits that nether Katoh nor Ito nor a combination thereof provide for, as specified in claim 1 of the instant invention:

1. forming a first network of nitride filled trenches in a first level of dielectric, the first level of dielectric having been deposited on the surface of the substrate
2. forming a second network of nitride filled trenches in a second level of dielectric, the second level of dielectric having been deposited on the surface of the first level of dielectric, whereby the second network of nitride filled trenches is in physical contact with and intersects with the first network of nitride filled trenches
3. depositing a first thin layer of oxide over the surface of the second layer of dielectric
4. etching openings in the first thin layer of oxide, the openings to align with the intersects between the first network

of nitride filled trenches and the second network of nitride filled trenches

5. removing the nitride from the second network of trenches and removing the nitride from the first network of trenches, and

6. depositing a second thin layer of oxide over the surface of the first thin layer of oxide thereby closing the openings in the first thin layer of oxide.

Applicant kindly suggests, based on the above presented arguments, that claims 1 and 11, and dependent claims 2-6 and 16-20, are unique and therefore patentable.

Some of the more salient differences between the instant invention and Katoh in view of Ito are summarized below:

- Katoh provides for the creation of crossing points for interconnections of semiconductor devices, the instant invention forms (mechanically stable) air gaps between metal lines,
- Fig. 1 of Katoh shows a first level interconnect (level 1) over which a second level (level 6) of interconnect is created and separated by the interconnections of insulating film; the instant invention, creates trenches in overlying layers of dielectric, the trenches are filled with air

- the metal interconnects of the instant invention are separated by a compound layer of dielectric, due to the special process of the invention the trenches are filled with air
- the conductive layers of interconnects of the instant invention are separated by (multiple) layers of dielectric in order to create a dielectric of low dielectric constant; by contrast, the conductive layers of the Katoh invention are overlying and perpendicularly intersecting and must be separated by an insulating film for the obvious reason that the overlying conductive layers would otherwise form electrical shorts there-between

In neither Katoh nor Ito is any reference made to creating overlying and perpendicularly intersecting trenches that are processed so that these trenches can be vacated of the therein contained semiconductor material. Katoh creates overlying layers of metal that perpendicularly intersect and are (by necessity) separated by a layer of insulation. Ito creates overlying layers of metal that are separated and supported by insulating posts. In neither Katoh nor Ito for instance is used a first and a second layer of oxide, the first to enable creating holes there-through so that the disposable material can be removed from the

trenches, the second to close the created air space after the trenches have been opened. Neither the trenches as used by the instant invention nor the creation of air spaces inside a layer of dielectric that separates interconnect traces, nor the steps of first creating openings (to remove the material contained in the trenches) and the closing of these openings overlying the trenches is provided by either Katoh and Ito nor is any reference thereto provided by either one of these inventions or by the combination thereof.

Claim 11 is specified in order to provide that the process of the invention can be applied using another material, other than nitride, that can also be removed from the trenches that have been created in the overlaying layers of dielectric. Claim 11 is therefore required to completely specify the method of the invention.

Regarding claims 2 and 3, these claims are required to provide further detail that relates to the independent claim thereof. It is clear that some processing steps that are part of the invention, such as providing a semiconductor substrate, may also be used for other semiconductor processing steps. This commonality however does not deny or affect the originality of the instant invention. The specification that is provided in

claims 2 and 3 completes the specification of the associated independent claim 1, without claims 2 and 3 the independent claim 1 may be open to dual and ambiguous interpretation.

Claim 6 is of importance in order to further highlight and claim that the invention can be applied for the creation of a layer of dielectric that separates adjacent layers of interconnect traces even where these interconnect traces are relatively far removed from each other. In this case openings of high-aspect ratio must be created through the interposed layers of dielectric. In view of the increased miniaturization of semiconductor devices, and the increased use of openings of high-aspect ratio, this claim takes on added significance for the era of sub-micron devices.

The repetition of claims 16- 20 is provided since these claims relate to and are provided in support of a different independent claim, that is claim 11, and does not, as the original claims 4-8, relate to the therewith associated independent claim 1.

ARGUMENTS IN SUPPORT OF claims 9-10, 12-14, 21-24 being patentable over Katoh (US Patent 5,141,896) and Ito (US Patent 6,297,145 B1) in view of Havemann et al. (US Patent 5,461,003).

The relative merits of Katoh (US Patent 5,141,896) and Ito (US Patent 6,297,145 B1) relating to the instant invention have been discussed supra and do therefore not need to be repeated at this time. These relative merits as argued supra are hereby included by reference thereto.

Havemann et al. forms multi-level layers of interconnect whereby air gaps are formed between adjacent interconnect traces.

Havemann et al. does not provide for:

- creating overlying layers of insulating material
- etching a first network and a second network of trenches in respectively the first and the second layer of insulating material after these layers have been deposited, whereby the trenches created in the overlying layers of insulating materials intersect under an angle, whereby this angle is measured as an angle created between a first intersection and a second intersection, the first intersection being an intersection of a first plane of a sidewall of a trench pertaining to a first network of trenches (overlying a semiconductor substrate) and the surface of a semiconductor substrate, the first plane having been extended towards the

surface of the semiconductor substrate to enable intersection therewith, the second intersection being an intersection of a second plane of a sidewall of a trench pertaining to a second network of trenches (overlying a semiconductor substrate) and the surface of the semiconductor substrate, the second plane having been extended towards the surface of the semiconductor substrate to enable intersection therewith

- filling the created trenches with a disposable material such as nitride
- depositing a first layer of oxide over the surface of the created layers of insulating material
- creating openings through the first layer of oxide that are aligned with the intersects of the first network and the second network of trenches
- removing the disposable material from the trenches in both the first and the second layer of insulating material, and
- depositing a second layer of oxide over the surface of the created layer of insulating material, thereby closing the openings that have been created through the first layer of oxide.

For all of these differences, the invention that is provided by Havemann et al., even if that invention has one or more

dependent processing steps in common with the instant invention, does not remove or affect the originality of the instant invention. Most notably, Havemann et al. remove a layer of disposable semiconductor material through a layer of porous dielectric material. Havemann et al. does created air gaps between adjacent and essentially parallel interconnect traces, the instant invention provides a layer of dielectric in which air trenches have been formed while the layers of interconnect metal are adjacent to the layer of dielectric.

Claims 9 and 10 specify further treatment that can be applied to the layers of dielectric that are used for the process of the invention. These special treatments are not basic to the process of the invention in which case these special treatments would have been included as part of an independent claim of the invention. Because of this and because these steps of process treatment are as yet important to the complete process of the invention (baking and curing of a layer of dielectric can significantly alter the behavior of a layer of dielectric in the processing stream of the instant invention), claims 9 and 10 have been provided. Under the Havemann et al. invention these steps may be applied but, if so, they are applied as part of a completely different processing sequence.

Claim 12 specifies the disposable solid layer comprising polymer, a material that is also applied by Haveman et al. Here too however the method and processing steps that are provided by Haveman et al. differ significantly from the method and processing steps of the instant invention, as has been highlighted in detail above. The commonality therefore of the use of polymer between the two inventions does not in any way provide commonality between the Havemann et al. invention and the instant invention, no more than for instance the common use of a temperature or a pressure would make two different inventions identical or even similar.

Claims 13-15 address aspects of removal of the disposable solid layer, a removal that is performed in a construct that is completely different from any of the here referred to constructs. It stands to reason that the combination of the creation of the openings in the first layer of oxide (overlying the layers of insulating material) and the removal of the (removable) material from the created trenches is not by itself an "obvious" step. Parameters of design (dimensions of the opening that are created, thickness of the layers of insulating material, the width and depth of the created trenches) have a significant effect on how the material can be removed from the trenches. In order to remove any ambiguity in this and in order

to specify the limitations of these combinations, the process of the removal of the disposable solid is critical and must therefore be specified in all its possibilities. Claims 13-15 provide these specifications.

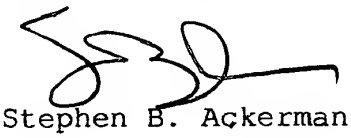
Claims 20 and 21 relate to a different independent claim than the previous claims, which have the same format. Since the independent claims (claim 1 and claim 11) are different, claims 20 and 21 must again be provided in order to avoid inadequate specification of independent claim 11.

Claim 23 provides for "deposing a layer of metal on the surface of said substrate" and "etching said layer of metal to form metal leads" over a semiconductor surface, as opposed to claim 1 wherein "said semiconductor substrate has been provided with points of electrical contact". Claim 23 therefore adds a level of complexity to the invention. Claim 24 has been amended as previously addressed for claims 4 and 5, as have claims 16 and 17.

For all of the above highlighted reasons, it is respectfully submitted that claims 1-14 and claims 16-24 should be allowed over Katoh (US Patent 5,141,896) and Ito (US Patent 6,297,145 B1). It is further respectfully submitted that claims 9-10, 12-

14 and 21-24 should be allowed over Katoh (US Patent 5,141,896) and Ito (US Patent 6,297,145 B1) in view of Havemann et al. (US Patent 5,461,003).

Respectfully submitted,



Stephen B. Ackerman (Reg. No 37,761)

ADDENDUM

The Claims outstanding in this application for United States Patent are as follows:

1. A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate whereby the surface of said semiconductor substrate has been provided with points of electrical contact;

forming a first network of nitride filled trenches in a first level of dielectric said first level of dielectric having been deposited on the surface of said substrate;

forming a second network of nitride filled trenches in a second level of dielectric said second level of dielectric having been deposited on the surface of said first level of dielectric whereby furthermore said second network of nitride filled trenches is in physical contact with and intersects with said first network of nitride filled trenches;

depositing a first thin layer of oxide over the surface of said second layer of dielectric;

etching openings in said first thin layer of oxide said openings to align with said intersects between said first

network of nitride filled trenches and said second network of nitride filled trenches;

removing said nitride from said second network of trenches furthermore removing said nitride from said first network of trenches; and

depositing a second thin layer of oxide over the surface of said first thin layer of oxide thereby closing said openings in said first thin layer of oxide.

2. The method of claim 1 wherein said forming a first network of nitride filled trenches in a first level of dielectric is:

depositing a first layer of dielectric over the surface of said substrate;

patterning and etching said first layer of dielectric thereby creating a first network of trenches in said first layer of dielectric;

depositing a first layer of nitride over the surface of said first layer of dielectric thereby including said first network of trenches; and

polishing said first layer of nitride thereby essentially removing said first layer of nitride from the surface of said first layer of dielectric.

3. The method of claim 1 wherein said forming a second network of nitride filled trenches in a second level of dielectric is:

depositing a second layer of dielectric over the surface of said first layer of dielectric thereby including said first layer of nitride;

patterning and etching said second layer of dielectric thereby creating a second network of trenches in said second layer of dielectric;

depositing a second layer of nitride over the surface of said first layer of dielectric thereby including said second network of trenches; and

polishing said second layer of nitride thereby essentially removing said second layer of nitride from the surface of said second layer of dielectric.

4. The method of claim 1 wherein said first network of trenches intersects said second network of trenches under an angle of about 90 degrees, said angle being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said first network of trenches and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said

second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said second network of trenches and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

5. The method of claim 1 wherein said first network of trenches intersects said second network of trenches under an angle other than 90 degrees, said angle being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said first network of trenches and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said second network of trenches and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

6. The method of claim 1 with the additional step of further extending the thickness of the combined said first thin layer of oxide and said second layer of oxide thereby enabling the

creation of openings of high aspect ratio in the extended layer of oxide combined with said first layer and said second layer of dielectric.

7. The method of claim 6 with the additional step of creating a network of metal interconnect lines on the surface of said extended layer of oxide.

8. The method of claim 1 with the additional step of forming A network of interconnect lines on the surface of said second thin layer of oxide.

9. The method of claim 1 with the additional steps of baking said first level of dielectric and/or said second level of dielectric said baking at a temperature between about 150 and 300 degrees C.

10. The method of claim 1 with the additional steps of curing said first level of dielectric and/or said second level of dielectric at an elevated temperature said curing at a temperature in excess of about 300 degrees C.

11. A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate whereby the surface of said semiconductor substrate has been provided with points of electrical contact;

forming a first network of trenches in a first level of dielectric said first level of dielectric having been deposited on the surface of said substrate whereby said first network of trenches is filled with a disposable solid layer, creating a first network of disposable solid filled trenches;

forming a second network of trenches in a second level of dielectric said second level of dielectric having been deposited on the surface of said first level of dielectric whereby said second network of trenches is in physical contact with and intersects with said first network of a disposable solid filled trenches whereby furthermore said second network of trenches is filled with a disposable solid layer, creating a second network of disposable solid filled trenches;

depositing a first thin layer of oxide over the surface of said second layer of dielectric;

etching openings in said first thin layer of oxide said openings to align with said intersects between said first network of trenches and said second network of trenches;

removing said disposable solid layer from said second network of trenches furthermore removing said disposable solid layer from said first network of trenches; and

depositing a second thin layer of oxide over the surface of said first thin layer of oxide thereby closing said openings in said first thin layer of oxide.

12. The method of claim 11 wherein said disposable solid layer is a polymer and whereby said removing said disposable solid layer is exposing said substrate to O_2 oxygen plasma thereby evaporating said disposable solid layer.

13. The method of claim 11 wherein said removing said disposable solid layer is introducing a solvent to said substrate thereby dissolving said disposable solid layer.

14. The method of claim 11 wherein said removing said disposable solid layer is heating said substrate thereby evaporating said disposable solid layer.

15. Please cancel claim 15.

16. The method of claim 11 wherein said first network of trenches intersects said second network of trenches under an angle of about 90 degrees, said angle being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane

of a sidewall of a trench pertaining to said first network of trenches and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said second network of trenches and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

17. The method of claim 11 wherein said first network of trenches intersects said second network of trenches under an angle other than 90 degrees, said angle being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said first network of trenches and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said second network of trenches and the surface of said semiconductor substrate, said second plane having been extended towards said

surface of said semiconductor substrate to enable intersection therewith.

18. The method of claim 11 with the additional step of further extending the thickness of the combined said first thin layer of oxide and said second layer of oxide thereby enabling the creation of openings of high aspect ratio in the extended layer of oxide combined with said first layer and said second layer of dielectric.

19. The method of claim 18 with the additional step of creating a network of metal interconnect lines on the surface of said extended layer of oxide.

20. The method of claim 11 with the additional step of forming a network of interconnect lines on the surface of said second thin layer of oxide.

21. The method of claim 11 with the additional step of baking said first level of dielectric and/or said second level of dielectric said baking at a temperature between about 150 and 300 degrees C.

22. The method of claim 11 with the additional step of curing said first level of dielectric and/or said second level of dielectric at an elevated temperature said curing at a temperature in excess of about 300 degrees C.

23. A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate;

depositing a layer of metal on the surface of said substrate;

etching said metal layer in a pattern to form metal leads, said metal leads running in a Y-direction said metal leads furthermore having top surfaces;

depositing a first layer of dielectric over the surface of said substrate thereby including said metal leads;

creating trenches in said first level of dielectric said trenches running in a X-direction;

filling said trenches in said first layer of dielectric with a first layer of nitride or another disposable solid;

depositing a second layer of dielectric over the surface of said first layer of dielectric thereby including said first layer of nitride or another disposable solid;

creating trenches in said second level of dielectric said trenches running in a Y-direction said trenches furthermore

having intersects with said trenches created in said first layer of dielectric;

filling said trenches in said second layer of dielectric with a second layer of nitride or another disposable solid;

depositing a first thin layer of oxide over the surface of said second layer of dielectric thereby including the surface of said second layer of nitride or other disposable solid;

etching openings in said first thin layer of oxide said openings to align with said intersects between said trenches created in said first level of dielectric and said trenches created in said second layer of dielectric;

removing said second layer of nitride or other disposable solid from said trenches created in said second layer of dielectric furthermore removing said first layer of nitride or other disposable solid from said trenches created in said first layer of dielectric thereby creating a network of trenches in said first layer of dielectric and in said second layer of dielectric whereby said trenches in said first layer of dielectric intersect said trenches in said second layer of dielectric under an angle of about 90 degrees, said angle of about 90 degrees being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said trenches created in said

first level of dielectric and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said trenches created in said second layer of dielectric and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith; and

depositing a second thin layer of oxide over the surface of said first thin layer of oxide thereby closing off said openings in said first thin layer of oxide.

24. The method of claim 23 wherein said whereby said trenches in said first layer of dielectric intersect said trenches in said second layer of dielectric under an angle other than 90 degrees, said angle of about 90 degrees being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said trenches created in said first level of dielectric and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an

intersection of a second plane of a sidewall of a trench pertaining to said trenches created in said second layer of dielectric and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

Claims 25-28. Please cancel claims 25-28.